

**What Is Claimed Is:**

1           1. A memory system comprising:  
2           a memory array containing a first plurality of cells, each of first plurality of cells  
3 storing a corresponding one of a plurality of data values;  
4           a decoding circuit selectively coupling a first cell to a bit line according to an access  
5 address, wherein said first cell is comprised in said plurality of cells; and  
6           a sense amplifier determining whether a current path is present on said bit line, said  
7 sense amplifier generating a first logical value as an output if said current path is present on  
8 said bit line and another logical value as said output otherwise, wherein said output represents  
9 a data value stored in said first cell.

1           2. The memory system of claim 1, wherein said first cell is designed to provide an  
2 open path to said bit line if said another logical value is stored and a closed path to said bit  
3 line if said first logical value is stored.

1           3. The memory system of claim 2, wherein said sense amplifier comprises:  
2           a first transistor having a gate terminal connected to a sense enable signal;  
3           a second transistor and a third transistor forming a current mirror, a drain terminal of  
4 each of said second transistor and said third transistor being connected to a source terminal  
5 of said first transistor, a gate terminal of said second transistor being connected to a gate  
6 terminal of said third transistor, said gate terminal of said second transistor also being  
7 connected to a source terminal of said second transistor at a first node, said bit line also being  
8 connected to said first node;

9 a fourth transistor having a gate terminal connected to said sense enable signal, a drain  
10 terminal of said fourth transistor being connected to said first node;

11 a resistor being connected to a source terminal of said third transistor at a second  
12 node; and

13 an inverter having an input coupled to said second node, wherein an output of said  
14 inverter represents said output of said sense amplifier.

1 4. The memory system of claim 3, wherein each of said first transistor, said second  
2 transistor, and said third transistor comprises a PMOS transistor, and said fourth transistor  
3 comprises a NMOS transistor, a drain terminal of said first transistor being connected to a  
4 supply voltage, a source terminal of said fourth transistor being connected to said ground, and  
5 a second end of said resistor also being connected to said ground.

1 5. The memory system of claim 4 wherein each of said plurality of cells comprises  
2 a transistor, said transistor being programmed to store one logic level if said bit line is  
3 connected to a drain terminal of said transistor and another logic level otherwise.

1 6. The memory system of claim 5, wherein said memory array comprises a compiler  
2 memory.

1 7. The memory system of claim 6, wherein each of said plurality of data values  
2 comprises a bit.

1           8. The memory system of claim 1, wherein said memory array is provided in the form  
2 of a plurality of rows and a plurality of columns, said decoding circuit comprising:  
3           a row decoder to select one of said plurality of rows; and  
4           a column decoder to select one of said plurality of columns.

1           9. The memory system of claim 1, wherein said memory array comprises an actual  
2 memory array.

1           10. The memory system of claim 1, further comprising a latch coupled to said output  
2 of said sense amplifier.

1           11. The memory system of claim 1, wherein said sense amplifier is implemented  
2 without using a reference signal which may be used for comparison with said current to  
3 determine the value of said one of said plurality of data values to be provided on said bit line.